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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,171	02/16/2004	Wen-Chin Lin	24061.163 (TSMC2003.0276)	1738

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EXAMINER	
SOFOCLEOUS, ALEXANDER	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,171	LIN ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/17/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *EAST search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Request for Continued Examination filed May 17, 2006, and the Information Disclosure Statement filed May 17, 2006.

2. Claims 10-14, 17-24 are pending in the case. Claim 10, 17, and 18 are independent claims.

Information Disclosure Statement

3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on May 17, 2006. This IDS has been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 10-14, 17, and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa U.S. Patent Application Publication No. 2002/0034117A1 in view of Sharma et al. (U.S. Patent Application Publication 2003/0117840).**

Regarding independent claim 10, Okazawa shows word lines (Fig. 4 MW1, MWm]), bit lines crossing the word lines (Fig. 4 [MB1, MBn]), a first set of switches

coupled to the corresponding bit line (Fig. 4 [BT11]), a second set of switches coupled to the corresponding word line (Fig. 4 [WT11]), and memory cells (Fig. 4 [C]) that are magnetic tunnel junction, or MTJ, devices (Paragraph 0011) including: a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

Each of the plurality of MTJ cells are positioned at crossing points of a bit line and a word line; and each of the MTJ cells is connected between the switch at the corresponding crossing bit line and the switch at the corresponding crossing word line (see Fig. 4).

Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors.

Sharma et al. disclose the provision of diodes as replacements for transistors for the purpose of blocking parasitic (sneak) currents.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Sharma et al. to the teachings of Okazawa such that the diodes are used instead of transistors for the purpose of blocking parasitic currents (see Sharma et al. paragraph 0051).

Regarding dependent claim 11, Okazawa shows that the total number of transistors is equal to the total number of plurality of word lines and the plurality of bit lines (see Fig. 4).

Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors.

Sharma et al. disclose the provision of diodes as replacements for transistors for the purpose of blocking parasitic (sneak) currents.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Sharma et al. to the teachings of Okazawa such that the diodes are used instead of transistors for the purpose of blocking parasitic currents (see Sharma et al. paragraph 0051).

Regarding dependent claim 12, Okazawa shows that the total number of cells is equal to the number of plurality of word lines times the number of plurality of bit lines (see Fig. 4).

Regarding dependent claim 13 and 14, Okazawa teaches that the memory array is an "m" x "n" matrix array, which denotes implicit variability of array dimensions (as discussed supra with respect to claims 8-9); hence 2 bit lines x 3 word lines and 3 bit lines x 3 word lines arrays are anticipated.

Regarding independent claim 17, Okazawa shows a MRAM array comprising:

a first word line (Fig. 4 [MW1]);

a second word line (Fig. 4 [MWm]);

a first bit line crossing the first word line and second word lines (Fig. 4 [MB1]);

a second bit line crossing the first word line and second word lines (Fig. 4 [MBn]);

a first transistor coupled to the first bit line (Fig. 4 [BT11]);

a second transistor coupled to the second bit line (Fig. 4 [BT1n]);

a third transistor coupled to the first word line (Fig. 4 [WT11]);

a first MTJ memory cell (Fig. 4 [C selected by BT11 and WT11]) is connected between the first transistor (Fig. 4 [BT11]) and the third transistor (Fig. 4 [WT11]), the first MTJ including:

a pinned layer (Fig. 1A [12]);

a free layer (Fig. 1A [14]);

and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

a second MTJ memory cell (Fig. 4 [C selected by BT1n and WT11]) is connected between the second transistor (Fig. 4 [BT1n]) and the third transistor (Fig. 4 [WT11]), the second MTJ including:

a pinned layer (Fig. 1A [12]);

a free layer (Fig. 1A [14]);

and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors.

Sharma et al. disclose the provision of diodes as replacements for transistors for the purpose of blocking parasitic (sneak) currents.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Sharma et al. to the teachings of Okazawa such that the diodes are used instead of transistors for the purpose of blocking parasitic currents (see Sharma et al. paragraph 0051).

It is further apparent, with respect to the above stated modification, that the diodes (replacing transistors BT11, BT1n, WT11) would need to be oriented to allow current to pass from the bit line through the memory cell to the word line; therefore, the diode orientation limitations (first MTJ connected between first diode's cathode and third diode's anode and second MTJ connected between second diode's cathode and third diode's anode) is met.

Regarding independent claim 18, Okazawa shows a first bus (Fig. 4 [BSL1]) associated with a plurality of first conductive lines (Fig. 4 [MW1, MWm]) and a second bus (Fig. 4 [WSL1]) associated with a plurality of second conductive lines (Fig. 4 [MB1, MBn]).

A plurality of first switches (Fig. 4 [BT11, BT1n]) couples the first bus (Fig. 4 [BSL1]) to the second conductive lines (Fig. 4 [MB1, MBn]) and a plurality of second switches (Fig. 4 [WT11, WT1m]) connects the second bus (Fig. 4 [WSL1]) to the first conductive lines (Fig. 4 [MW1, MWm]).

A plurality of magnetic tunnel junction memories (Fig. 4 [C]) are positioned where one first conductive line and one second conductive line crosses (see Fig. 4 [MW1 and MB1]) wherein each of the plurality of MJT memories is connected between a first switch (see Fig. 4 [BT11]) at a corresponding second conductive line (see Fig. 4 [MB1]) and a second switch (see Fig. 4 [WT11]) at a corresponding first conductive line (see Fig. 4 [MW1]).

Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors.

Sharma et al. disclose the provision of diodes as replacements for transistors for the purpose of blocking parasitic (sneak) currents.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Sharma et al. to the teachings of Okazawa such that the diodes are used instead of transistors for the purpose of blocking parasitic currents (see Sharma et al. paragraph 0051).

Regarding independent claim 19, each of the MJT memories includes a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

Regarding dependent claim 20, Okazawa shows that the total number of first and second switches is equal to the total number of plurality of first and second conductive lines (see Fig. 4).

Regarding dependent claim 21, Okazawa shows that the total number of MJT cells is equal to the product of the number of plurality of first conduction lines and the number of plurality of second conductive lines (see Fig. 4).

Regarding independent claim 22, Okazawa shows a plurality of segments (Fig. 4 [SW11, SW1m, SB11, SB1n]), wherein each segment includes at least two of the plurality of MTJ memories (see Fig. 4).

Regarding independent claim 23, Okazawa shows a plurality of segments (Fig. 4 [SW11, SW1m, SB11, SB1n]) that are separated by field effect transistors (Fig. 4 [WT11, WT1m, BT11, BT1n]).

Regarding dependent claim 24, Okazawa shows the segments (Fig. 4 [SW31, SW3m]) are separated by field effect transistors.

Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors.

Sharma et al. disclose the provision of diodes as replacements for transistors for the purpose of blocking parasitic (sneak) currents.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Sharma et al. to the teachings of Okazawa such that the diodes are used instead of transistors for the purpose of blocking parasitic currents (see Sharma et al. paragraph 0051).

6. **Claims 10-12, 14, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (U.S. Patent 5,640,343) in view of Perner et al. (U.S. Patent 6,937,509).**

Regarding independent claims 10 and 18 (and dependent claim 19), Gallagher et al. show an MRAM memory array (Fig. 2) comprising:

word lines (Fig. 2 [1, 2, 3]);

bit lines (Fig. 2 [4, 5, 6]) crossing word lines (Fig. 2 [1, 2, 3]);

second diodes (Fig. 2 [7]), each second diode comprising:

an anode (see Fig. 2 [7]);

and a cathode coupled to the corresponding word line (see Fig. 2 [7 with respect to 1]); and

magnetic tunnel junction memories (Fig. 2 [8]) including:

a pinned layer (Fig. 1C [20]);

a free layer (Fig. 1C [24]); and

a non-magnetic layer (Fig. 1C [22]) located between the pinned layer (Fig. 1C [20]) and the free layer (Fig. 1C [24]); each magnetic tunnel junction (Fig. 2 [8]) being connected between the bit line a second diode at the corresponding crossing word line (see Fig. 2 [8 with respect to 1, 4, and 7]).

Gallagher et al. are silent with respect to a first diode with its cathode connected to a bit line; and the MTJ being connected between the first diode and the second diode.

Perner et al. show first diodes (Fig. 6 [25]) each first diode comprising:

a cathode (see Fig. 6 [25]);

and an anode coupled to the corresponding bit line (see Fig. 6 [25 with respect to 16]); and

each MTJ (see Fig. 6 [18] with respect to column 2, lines 58-62) being connected between a first diode at the corresponding crossing bit line and a word line (see Fig. 6 [18 with respect to 14, 16, and 25]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Perner et al. to the teachings of Gallagher et al. such that an array of MTJ cells are located between first diodes connected to the bit lines (from Perner et al.) and second diodes connected to the word lines (from Gallagher et al.) for the purpose of reliably isolating the selected resistive memory cells in order to

prevent sneak currents (see Perner et al. column 1, lines 50-53 with respect to lines 41-43, 46-49). Further motivation to perform the above stated modification is evidenced by the fact that both Gallagher et al. and Perner et al. show magnetic memories with word lines, bit lines, and diodes to prevent sneak currents and are commonly classified in class 365 (static memories).

Regarding dependent claims 11 and 20, the combination of Gallagher et al. and Perner et al. would result in one diode per word line (as per Gallagher et al.) and one diode per bit line (as per Perner et al.); therefore, the total number of diodes or switches is equal to the number of first (word line) and second (bit line) conductive lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Perner et al. to the teachings of Gallagher et al. such that an array of MTJ cells are located between first diodes connected to the bit lines (from Perner et al.) and second diodes connected to the word lines (from Gallagher et al.) for the purpose of reliably isolating the selected resistive memory cells in order to prevent sneak currents (see Perner et al. column 1, lines 50-53 with respect to lines 41-43, 46-49). Further motivation to perform the above stated modification is evidenced by the fact that both Gallagher et al. and Perner et al. show magnetic memories with word lines, bit lines, and diodes to prevent sneak currents and are commonly classified in class 365 (static memories).

Regarding dependent claims 12 and 21, Gallagher et al. show the number of MTJ cells is the product of word lines and bit lines (see Fig. 2: 3 bit lines [4, 5, 6], 3 word lines [1, 2, 3], and 9 MTJ [8]).

Regarding dependent claim 14, Gallagher et al. show three word lines (Fig. 2 [1, 2, 3]) and three bit lines (Fig. 2 [4, 5, 6]).

Conclusion

It is noted that in prior office action (dated February 17, 2006), claims 10-14, and 17-24 were indicated as allowable; however, in light of newly found art, new rejections are presented.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Tang et al. (U.S. Patent 6,885,577) and Lin et al. (U.S. Patent Application Publication 2005/0243598).

Tang et al. show magnetic memories with diodes connected from the bit lines to the MRAM cells.

Lin et al., commonly assigned art, show segmented magnetic memory.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

7/7/06

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